Hardware/Software Codesign Lab 4

1. Answer the following question:
2. Specify the location(s) for the DDR3 Controller and DDR3 memory: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.

DDR3 Controller inside Zynq PS, hard core.

DDR3 Memory outside Zynq.

1. Specify the location(s) for the AXI-BRAM Controller and BRAM in this lab: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.

Both inside Zynq PL, soft core.

1. Specify the locations assigned to the code, data, stack and heap section of your software executable for the two linker script settings tested in the lab.

First in DDR3 memory, second in BRAM

1. List all the external peripherals in the embedded system you build in this lab.

Leds, push buttons, dip switches, DDR3 memory UART.